

# BeamFormer ASIC in UHF-L band for the Square Kilometer Array international project

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**Abstract**— An implementation of a beamformer Application Specific Integrated Circuit (ASIC) is described in this paper, for the European SKA demonstrator project EMBRACE (Electronic Multi-Beam Radio-Astronomy ConcEpt), using the QUBiC4G 0.25  $\mu\text{m}$  Silicon Germanium process of NXP. This process is qualified as a high-performance technology to design a RF ASIC in the frequency band [400 MHz - 1600 MHz]. The chip is designed to form two antenna beams by means of phase-shift and amplitude control. The integrated circuit includes many differential functions such as low noise amplifiers, switches, polyphase filters, variable gain attenuators and a SPI interface for the digital control of all settings. The number of phase steps of this beamformer-chip (BFC) is 8 and their values are equal to 45 degrees equally distributed (360 degrees, 3 bits). Amplitude control of 5 dB with 8 steps equally distributed is implemented to accomplish a phase dependent amplitude variation of less than +/- 0.5 dB. The total power consumption of the beamformer-chip is 1 Watt with a supply voltage of 3.3 V. The differential input and output impedance matching is 100 ohms. The surface of BFC is 2.3x2.3 mm<sup>2</sup>.

This BFC designed by Nançay engineers has been a success and 4,700 of them were manufactured for the EMBRACE project [1].

## I. INTRODUCTION

The motivation for SKA comes from the necessity to detect faint emission from hydrogen gas in structures forming soon after the Big Bang, and in galaxies which formed from these structures. Hydrogen is the most abundant element in the Universe but detecting it in distant galaxies requires ultra-sensitive equipment [2].

The Square Kilometre Array will be a gigantic radio telescope. Building such an advanced and innovative instrument as SKA requires the development of new technology, such as integrated circuits for the reception and processing of signals. The microelectronics laboratory at the Nançay Radio Astronomy Facility has a head start on the international competition to develop these chips. Nançay engineers have designed a chip and 4,700 of them were manufactured for the first demonstrator EMBRACE, and are already working on the next phase, known as Aperture Array Verification Program (AAVP).

EMBRACE is the Electronic MultiBeam Radio Astronomy ConcEpt and it will be an aperture-plane phased-array using tiles of Vivaldi feed antennas. This concept was initially developed by ASTRON (the Netherlands Institute for Radio Astronomy) in which 72 elementary antennas are densely packed into a tile and connected with beam-forming circuitry.

A tile provides a physical collecting area of about one square metre. Two demonstrators will be built in Westerbok (Netherlands) and in Nançay (France) with a total collecting area of around 220 m<sup>2</sup>.

For cost reasons, analogue beamforming and RF combiners are used to limit the number of digital receivers. A higher integration density is required, compared to designed discrete prototypes, with a lower cost technology based on Silicon.

BeamFormer-Chip is the name given to this integrated circuit. This chip combines four input signals, coming from four antennas, into two independent beams. This ASIC uses NPN and CMOS transistors involving 0.25  $\mu\text{m}$  BiCMOS QUBiC4G technology from New Experience Philips (NXP).

## II. ARCHITECTURE

Four antennas including LNAs (not presented in this paper) are connected to the chip, in which two independent beams are generated by a beam-forming technique. The BFC architecture can be divided in four channels which generate two beams (Fig. 1). Each channel contains its own digital control circuit to set the phase states of the beams and a network which combines the desired signal stream with the others.

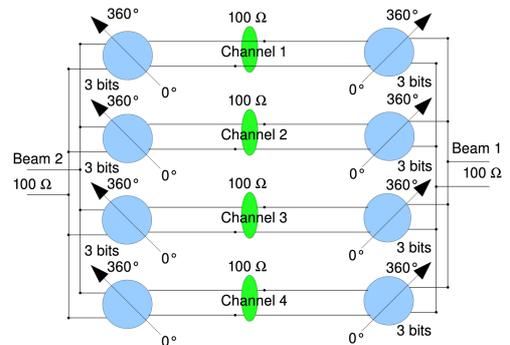


Fig. 1: Block diagram of BeamFormer-Chip

Fig. 2 shows the block diagram of a channel, which consists of gain and buffer stages, phasing and variable gain attenuator networks. The implementation of the BFC is differential. In addition to isolation from ground (differential topology), the motivation for implementing the differential concept is also the cancellation of the even intermodulation products  $IM_2, IM_4 \dots$  which is achieved by a proper differential design.

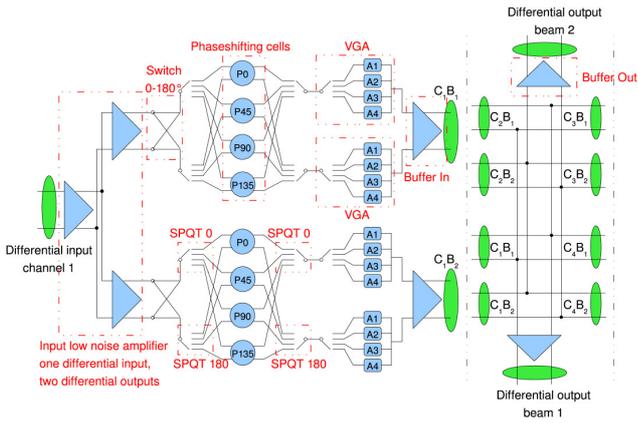


Fig. 2: Block diagram of one channel/one beam

### III. DESCRIPTION OF DIFFERENT PARTS

The first gain stage is a low noise amplifier which splits by two the input signal (Fig. 3). This is accomplished by a wide-band topology [3][4], to obtain an input impedance matching of  $100 \Omega$  differentials with a good compromise between the noise figure and the Output third-order Intercept Point (OIP3). The switch 0-180 generates a phaseshifting of 180 degrees or none (Fig. 4). Then a switch SPQT (Fig. 5) selects a desired phaseshifting of values 0, 45, 90, or 135 degrees. The four P0, P45, P90 and P135 cells which generate a phaseshifting are implemented with a RC polyphase filter [5]. The polyphase filter has been optimized with ADS from Agilent [7] and transformed in four different cells as shown in Fig. 6. This is different than a polyphase network [6] which generates four cardinal vectors 0, 90, 180 and 270 degrees, used to form the desired phase of the output signal by vector summation.

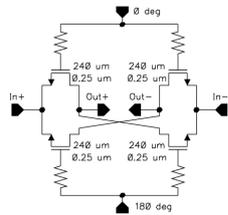


Fig. 5: Switch 0/180 degrees

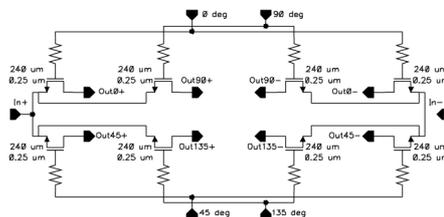


Fig. 4: Switch SPQT

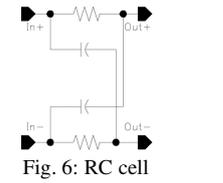


Fig. 6: RC cell

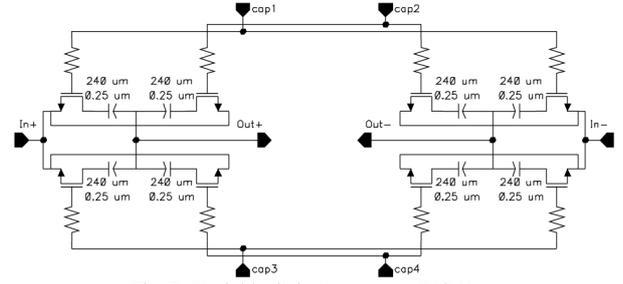


Fig. 7: Variable Gain Attenuator (VGA)

The Variable Gain Attenuator (VGA) (Fig. 7) creates a capacitive attenuation to equalize the level gain of each phaseshifting (if necessary). The use of capacitors is the best solution to stabilize the phase when a gain state is selected. The BufferIn (Fig. 8) combines the four channels to form one beam, with the output impedance matched with the input impedance of the BufferOut (Fig. 9).

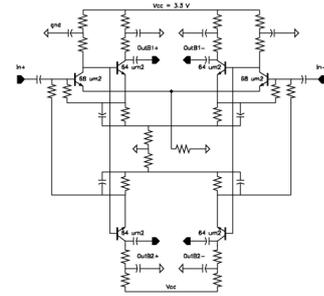


Fig. 3: Input low noise amplifier

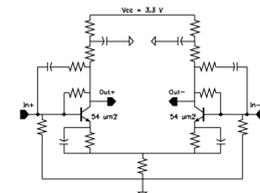


Fig. 8: BufferIn to combine

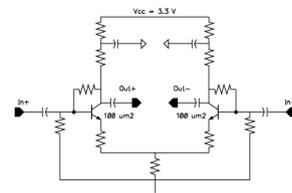


Fig. 9: BufferOut to combine

The differential output impedance matching of BufferOut is  $100 \Omega$ .

#### IV. SIMULATION RESULTS

The technology QUBiC4G 0.25  $\mu\text{m}$  SiGe of NXP has been used to design this complex chip. A photograph of the BFC is showned in Fig. 10. The die occupies an area of  $2.3 \times 2.3 \text{ mm}^2$ .

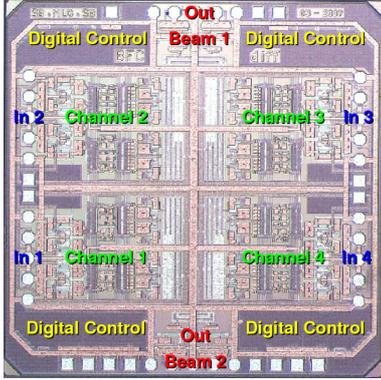


Fig. 10: Photograph of the BeamFormer-Chip

The Chip is mounted in a QFN48 package with ground paddle. This BFC has four inputs and two outputs and the small area justifies the choice of topologies. The electrical consumption of different parts are presented in Table 1.

TABLE 1 : POWER CONSUMPTION OF DIFFERENT PARTS

Cell	Power consumption mW	
	BFC	One channel
LNA 1 <sup>st</sup> Stage	49 x4 = 196	x1 = 49
LNA 2 <sup>nd</sup> Stage	52 x8 = 416	x2 = 104
BufferIn	26 x8 = 208	x2 = 52
BufferOut	98 x2 = 196	x0.5 = 49
Total	1014	254

The total power consumption of the BeamFormer-Chip is 1 W @ 3.3 Volts. The power consumption of one channel is 254 mW and one channel/one beam is 127 mW.

The simulated system Noise figure (NF) is 4.1 dB when the 4<sup>th</sup> gain state is selected, but it changes from 1.8 dB to 6.2 dB depending on the selected gain. The LNA's gain is not high enough to reduce this variation but it has been optimized to reduce the power consumption. The level gain (differential transmission coefficient  $s_{dd21}$ ) is 12 dB (4<sup>th</sup> gain state). The simulated OIP3 is higher than 1 dBm (one input to one output), so the value of Carrier to 3<sup>rd</sup> Order Intermodulation Ratio ( $C/I_3$ ) is about 58 dB @ input power = -40 dBm. Fig. 11 shows that the gain difference is smaller than 0.5 dB between all phase states.

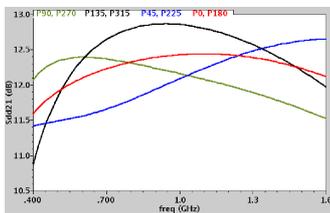


Fig. 11: Gain of different phases

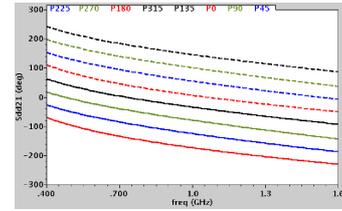


Fig. 12: Different phase states

In Fig. 13 we can see that VGA gives 8 gain states with identical steps between each gain state, except between the 4<sup>th</sup> and 5<sup>th</sup> gain state. In Fig. 14 we can see the phase difference between every gain state and the 1<sup>st</sup> gain state. The phase is independent from the gain state. At worst, this phase variation is from  $-4.2^\circ$  to  $2.3^\circ$ .

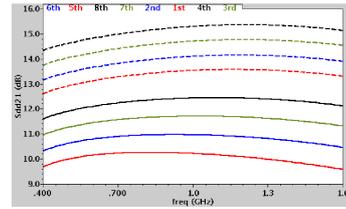


Fig. 13: Different gain states

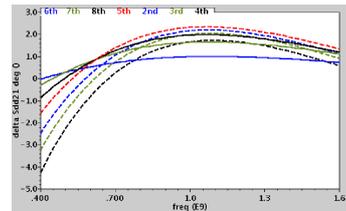


Fig. 14: Phase error/different gain states

#### V. MEASUREMENT RESULTS

Measurements of the BeamFormer-Chip agree with simulations, as can be seen by comparing Fig. 11-15, 12-16, 13-17 and 14-18.

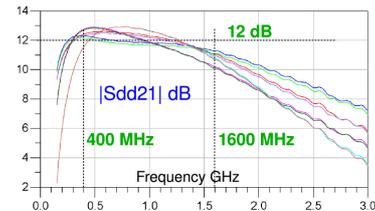


Fig. 15: Gain of different phases

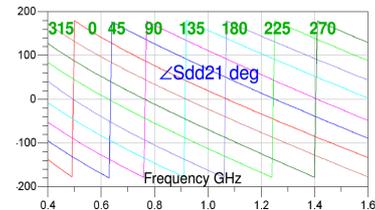


Fig. 16: Different phase states

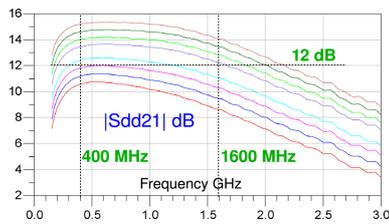


Fig. 17: Different gain states

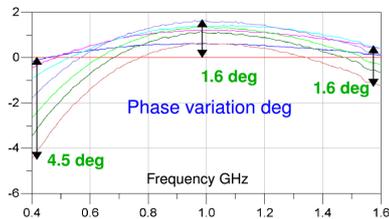


Fig. 18: Phase error/different gain states

Fig. 19 shows a very good measured differential input and output impedance matching on  $100 \Omega$ . The measured common mode (Fig. 20) is lower than  $-25$  dB in the frequency band. This allows good cancellation of the even intermodulation products  $IM_2$ ,  $IM_4$ , ...

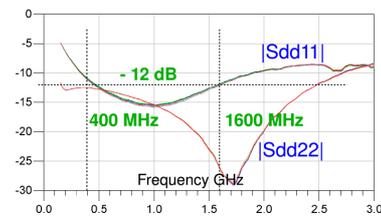


Fig. 19: Reflexion Coefficients

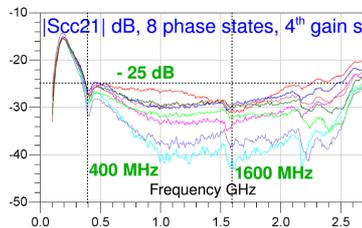


Fig. 20: Common mode rejection

The power consumption is 1.1 Watts. The system Noise figure is 4.0 dB when the 4th gain state is selected, the level gain  $Sdd_{21}$  is about 12 dB (4th gain state). The measured OIP3 is higher than  $-2$  dBm (one input to one output). It is different from the simulation due to the temperature sensitivity.

## VI. CONCLUSION

A SiGe ASIC with phase and amplitude control in UHF-L band for the Square Kilometer Array demonstrator project EMBRACE has been designed. The functionality of this prototype is proven by providing 4,700 BeamFormer-Chips for EMBRACE. Measurements are very good and precisely match simulations. It's an important result which shows that the process QUBiC4G 0.25  $\mu\text{m}$  SiGe of NXP is qualified as a

high performance technology to integrate a complex RF ASIC in this frequency band. In the wake of this success, the Nançay microelectronic team is working to further improve the performance of this chip by integrating a smaller phase step of 22.5 degrees, by increasing OIP3 or C/I3 with the same power consumption, and by using the newer process QUBiC4X SiGeC 0.25  $\mu\text{m}$  of NXP.

This result benefited from the advanced use of ADS software by Agilent.

## ACKNOWLEDGEMENT

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